REMARKS

Applicant is concurrently filing a Submission of Corrected Formal Drawings with this Amendment that include the drawing corrections approved in the Advisory Action dated November 30, 2001.

Applicant herein cancels claims 14, 16 and 20 without prejudice and/or disclaimer. Claim 20 was added by the Amendment Under 37 C.F.R. § 1.116 filed on November 15, 2001. Entry of claim 20 was requested in the Request for Continued Examination filed on January 15, 2002. However, the Examiner failed to enter and consider claim 20.

Applicant herein adds new claims 30-32. The new claims 30-32 are fully supported by the specification, and add no new matter. Support for new claims 30-32 can be found in Figures 9-14 and at page 27, line 4 to page 29, line 3 of the specification (see discussion below regarding 35 U.S.C. § 112, first paragraph rejection). No additional fees are believed to be necessary for these new claims. Entry and consideration of the new claims is requested.

1. Claim 24 has been withdrawn from consideration as being drawn to a non-elected embodiment. Applicant traverses the Examiner's withdrawal as being unnecessary and unsupportable. The subject matter of claim 24 is readable on the elected species, and, in fact, is discussed in the text that describes the elected species. *See* page 18, lines 20-23 of the specification. The Examiner has made no showing that claim 24 does not read on the elected species. Applicant requests that claim 24 be reinstated under 37 C.F.R. § 1.142(b).

2. Claims 27-29 stand rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification. Applicant traverses the rejection of claims 27-29, and insofar as the rejection applies to new claims 30-32, at least for the reasons set forth below.

A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. *See, e.g., In re Marzocchi*, 439 F.2d 220, 224 (CCPA 1971). The examiner has the initial burden of presenting by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. *In re Wertheim*, 541 F.2d 257, 263 (CCPA 1976).

The Examiner's rejection of claims 27-29 under 35 U.S.C. § 112, first paragraph is unreasonable in light of *Marzocchi* and *Wertheim*, as well as the guidelines set forth at MPEP § 2163.04. The Examiner simply states that the description would not convey to one skilled in the art that the inventor was in possession of the invention at the time the application was filed, and provides no support for his statement. Thus, Applicant believes that the Examiner has failed to make a *prima facie* case as required under MPEP § 2163.04 (I)(B).

Contrary to the Examiner's statement at page 2, numbered paragraph 3 of the Office Action dated March 14, 2002, the specification states that, for the first embodiment, the electrostatic protection element can be a bipolar transistor, a thyristor or a non-parasitic diode. *See* page 18, lines 3-6 of the instant specification. In the Office Action, there is no explanation as to why one of ordinary skill in the art would not understand that the inventor was in possession of the invention at the time of the filing of the application. It is well settled that patent need not teach, and preferably

omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991). The Examiner has not provided any detailed reasoning as to why the use of a bipolar transistor, a thyristor or a non-parasitic diode as an electrostatic protection element would not be understood by one of ordinary skill in the art.

In fact, if one of ordinary skill in the art reads the specification, it would be readily apparent that the inventor was in possession of the invention at the time of the filing of the application. To illustrate, the first embodiment of the invention (see Figure 1 of the instant application) and the third embodiment of the invention (see Figure 4 of the instant application) share an identical circuit structure vis-à-vis the electrostatic protection element (18) and the MOS capacitor (16). Figures 9 and 10 and the accompanying text describe the construction of a bipolar transistor (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 9 and 10; page 27, line 14 to page 28, line 14 of the instant specification. Figures 11 and 12 and the accompanying text describe the construction of a non-parasitic diode (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 11 and 12; page 28, line 15 to page 29, line 3 of the instant specification. Figures 13 and 14 and the accompanying text describe the construction of a thyristor (electrostatic protection element 18) and a MOS capacitor (16) for the third embodiment of the invention. *See* Figures 13 and 14; page 29, line 3 to page 30, line 2 of the instant specification. The reference numbers for the electrostatic protection element and MOS capacitor shown in Figure 1 are no different than the reference numbers for the electrostatic protection element and MOS capacitor shown in Figures 4 and 9-14. *See* 37 C.F.R. § 1.84(p)(4) (same reference numbers are used for identical parts in

different views). In sum, with respect to the elected embodiment, the written description and the drawings disclose an electrostatic protection element that can be a bipolar transistor, a thyristor or a non-parasitic diode.

Previously, the Examiner argued that the written description for a non-elected claim could not be used to provide support for an element of an elected claim. *See* Final Office Action dated August 15, 2001, page 5, numbered paragraph 6. However, it is clear that the electrostatic protection element (18) and the MOS capacitor (16) illustrated in Figure 1 are identical to the electrostatic protection element (18) and the MOS capacitor (16) depicted in Figure 4. These Figures are original, and have not been amended in any way. Applicant notes that the Examiner has not identified any relevant Federal Circuit case law, Title 37 C.F.R. section or MPEP section that supports his position. Thus, Applicant believes that the Examiner is being unreasonable that one skilled in the art of semiconductor manufacturing would not understand that a bipolar transistor, a thyristor or a non-parasitic diode could be used as the electrostatic protection element. Applicant requests that the Examiner withdraw the § 112, first paragraph rejection.

With respect to new claims 30-32, these new claims recite similar subject matter as claims 27-29, and Applicant believes that these new claims are definite for the same reasons as claims 27-29. The new claims 30-32 are readable on the elected species as well.

3. Claims 3, 8, 10, 12 and 13 stand rejected under 35 U.S.C. § 112, second paragraph as being indefinite.

As argued previously, the rejection of claims 3, 8, 10, 12 and 13 is premature. Claims 3, 8,

10, 12 and 13 are multiple dependent claims that depend from claims 1 and 2. Claim 1 was elected for prosecution on the merits and has been indicated as generic by the Applicant in the Response to Election of Species Requirement filed on March 21, 2001. The claims are not rendered indefinite because they depend from both elected and non-elected species. Therefore, it is unnecessary to consider the metes and bounds of claims 3, 8, 10, 12 and 13 with respect to claim 2. Claim 2 has been withdrawn from consideration, and the form of claims 3, 8, 10, 12 and 13 depending from non-elected claim 2 should simply be considered as withdrawn claims. The Examiner appears to be confusing an election of species requirement with a restriction requirement. At present, no burden has been placed on Applicant to file a divisional application with respect to the non-elected claims. Again, Applicant requests that the Examiner withdraw the §112 rejection as premature.

4. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. (U.S. Patent No. 4,456,939) in view of Miller (U.S. Patent No. 5,255,146).

The Examiner again acknowledges that Ozaki et al. fails to teach or suggest that the wire resistance of the ground potential wire between the ESD element connection point and the ground terminal is larger that the wire resistance of the ground potential wire between the ESD element connection point and the MOS capacitor connection point. *See* numbered paragraph 7, page 4 of the Office Action dated March 14, 2002. To overcome the deficiencies of Ozaki et al., the Examiner states that the positioning of the ESD element connection point on the ground potential wire relative to the MOS capacitor connection point on the ground potential wire would be a matter of design

choice within the skills of an artisan, and that computers are routinely used to design integrated circuit layouts. However, the Examiner is obligated to provide concrete evidence in the record to support his assertion that it is well within the skills of an artisan to find the optimum layout of the Applicant's device by using computers. *See In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001). The Examiner cannot simply reach conclusions based upon his own assessment of what would be basic knowledge or common sense. *Id.* Thus, Applicant maintains that nothing in Ozaki et al. teach or suggest the resistance relationship as recited in independent claims 1 and 21, and it would not be a matter of design choice. Finally, with respect to design choice, only the simple repositioning of isolated components has ever been found to be covered by the umbrella of "design choice" and not the specific arrangement of cooperative elements. *In re Japikse*, 86 U.S.P.Q. 70 (C.C.P.A. 1950)(the repositioning of an actuating switch from one physical location to another cannot be the basis of patentability for a hydraulic press).

As an alternative, the Examiner combines Ozaki et al. with Miller in order to overcome the acknowledged deficiencies of Ozaki et al. The combination of Ozaki et al. and Miller, however, fails to teach or suggest the invention recited in independent claims 1 and 21. Figure 2 of Miller depicts a plurality of ESD protection circuits 14 connected between a V_{DD} ring and a V_{SS} ring.

The combination of Ozaki et al. and Miller fails to teach or suggest that the wire resistance of a ground wire portion between an electrostatic protection element and a ground terminal is larger than a wire resistance of the ground wire portion between the electrostatic protection element and a MOS capacitor, as recited in independent claims 1 and 21. In Figure 2 of Miller and its accompanying text, there is no indication that the ESD protection circuit 14 is positioned relative

to a MOS capacitor such that the resistive relationship as recited in claim 1 is taught or suggested. The combination of references fails to show, however, the claimed resistance relationship between an electrostatic protection device and a capacitor, as recited in independent claims 1 and 21.

Applicant reminds the Examiner that the initial burden of establishing that a claimed invention is *prima facie* obvious rests on the USPTO. *In re Piasecki*, 745 F.2d 1468, 1472 (Fed. Cir. 1984). To make its *prima facie* case of obviousness, the USPTO must satisfy three requirements:

1. The prior art relied upon, coupled with the knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated to artisan to modify a reference or to combine references. *In re Fine*, 837 F.2d 1071, 1074 (Fed. Cir. 1988).
2. The proposed modification of the prior art must have had a reasonable expectation of success, and that determined from the vantage point of the artisan at the time the invention was made. *Amgen, Inc. v. Chugai Pharm. Co.*, 927 F.2d 1200, 1209 (Fed. Cir. 1991).
3. The prior art reference or combination of references must teach or suggest all the limitations of the claims. *In re Vaeck*, 20 U.S.P.Q.2d 1438, 1442 (Fed. Cir. 1991); *In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970).

The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, the nature of a problem to be solved. *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999). Alternatively, the motivation may be implicit from the prior art as a whole, rather than expressly stated. *Id.* Regardless if the USPTO relies on an express or an implicit showing of motivation, the USPTO is obligated to provide particular findings

related to its conclusion, and those findings must be clear and particular. *Id.* A broad conclusionary statement, standing alone without support, is not "evidence." *Id.; see also, In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

In addition, a rejection cannot be predicated on the mere identification of individual components of claimed limitations. *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000). Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *Id.*

The Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Miller. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied. Moreover, the Examiner has not pointed to any teaching or suggestion in Miller, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. The Examiner simply states that Figure 2 of Miller shows the claimed resistive relationship, without any further support as to how one of skill in the art would derive that teaching from Miller. Thus, the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness has not been satisfied either. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claims 1 and 21, as required by *Piasecki*.

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Miller, and Applicant further believes that claims 3, 8, 10, 12, 13, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

4. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. in view of Puar (U.S. Patent No. 4,786,956).

The Examiner combines Puar with Ozaki et al. in an attempt to overcome the deficiencies of Ozaki et al. with respect to the resistance relationship recited in independent claims 1 and 21. The Examiner alleges that Puar depicts an ESD circuit (16) being located closer to an integrated circuit (10) than to a ground terminal such that the ground wire resistance between the ESD circuit (16) and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit (16) and the ground connection point.

Again, Applicant submits that the Examiner has failed to make a *prima facie* case of obviousness as required by *Piasecki*. The Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Puar. The record simply lacks any discussion of motivation whatsoever. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied.

In addition, the Examiner has not cited any teaching or suggestion in Puar, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. The Examiner simply states that Figure 1 of Puar shows the claimed resistive relationship, without any further support as

to how one of skill in the art would derive that teaching from Puar. Puar is replete with diagrams of the ESD circuit (16), but there is no teaching or suggestion of the resistance relationship between an ESD element, a capacitor and a ground terminal as recited in independent claims 1 and 21. Moreover, the Examiner's statement that Figure 1 of Puar shows the claimed resistive relationship does not make sense, since no ground wire paths are even depicted. Applicant believes that the Examiner has failed to satisfy the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness as well. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claims 1 and 21, as required by *Piasecki*.

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Puar, and Applicant further believes that claims 3, 8, 10, 12, 13, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

5. Claims 1, 3, 8, 10, 12, 13, 21-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozaki et al. in view of Igarashi (U.S. Patent No. 4,656,491).

The Examiner combines Igarashi with Ozaki et al. in an attempt to overcome the deficiencies of Ozaki et al. with respect to the resistance relationship recited in independent claims 1 and 21. The Examiner alleges that Igarashi depicts an ESD circuit being located closer to an integrated circuit than to a ground terminal such that the ground wire resistance between the ESD circuit and the ground terminal is larger than the wire resistance between the ESD elements within the ESD circuit and the ground connection point.

Applicant submits that the Examiner has failed to make a *prima facie* case of obviousness as required by *Piasecki*. The Examiner has not made any findings on the record, as required by *Dembiczak*, as to why one of ordinary skill in the art would be motivated to combine Ozaki et al. and Igarashi. Again, the record simply lacks any discussion of motivation whatsoever. Thus, the motivation prong of a *prima facie* case of obviousness has not been satisfied.

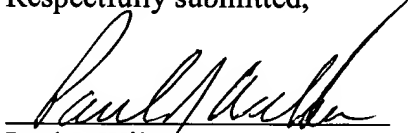
In addition, the Examiner has not cited any teaching or suggestion in Igarashi, when combined with Ozaki et al., that would teach or suggest the claimed resistance relationship between an electrostatic protection device and a capacitor recited in independent claims 1 and 21. In fact, the Figures cited by the Examiner show the opposite of the claimed resistive relationship. To illustrate, the resistor (R12) is connected between the transistors Q11-Q1n. *See* Fig. 4 of Igarashi. However, there is very little resistance between the ground terminal (103) and the transistor Q1n. This resistive relationship is opposite to the resistive relationship recited in independent claims 1 and 21. *See W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540 (Fed. Cir. 1983) (prior art reference must be considered in its entirety, including portions that would teach away from the claimed invention). Applicant believes that the Examiner has failed to satisfy the teaching or suggesting all the limitations prong of a *prima facie* case of obviousness as well, since it is apparent that the combination of Igarashi with Ozaki et al. discloses a resistive relationship that is opposite to the claimed resistive relationship. Therefore, Applicant maintains that the Examiner has not set forth a *prima facie* case of obviousness with respect to independent claim 1, as required by *Piasecki*.

Thus, Applicant believes that independent claims 1 and 21 are allowable over the combination of Ozaki et al. and Igarashi, and Applicant further believes that claims 3, 8, 10, 12, 13, 21-23 and 25-29 at least by virtue of their dependency from claims 1 and 21, respectively.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 14, 16 and 20 are canceled without prejudice and/or disclaimer.

The claims are amended as follows:

12. (*Twice Amended*) A semiconductor integrated circuit device according to any one of claims 1 or [and] 2, wherein said electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the gate of which are connected to said ground potential wire.

13. (*Twice Amended*) A semiconductor integrated circuit device according to any one of claims 4 or [and] 5, wherein said second electrostatic protection element is a MOS field effect transistor, the drain of which is connected to said power source wire, and the source and the gate of which are connected to said ground potential wire.

Claims 30-32 are added as new claims.